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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,807	10/29/2003	Masahiro Takenaka	4074-9	6780

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EXAMINER	
GUERRERO, MARIA F	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,807	TAKENAKA, MASAHIRO	
	Examiner	Art Unit	
	Maria Guerrero	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is the First Action on the merits.

Status of Claims

2. Claims 1-20 are pending.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Information Disclosure Statement

5. The information disclosure statement filed October 29, 2003 has been considered.

Duplicate Claims

6. Applicant is advised that should claims 4 and 14 be found allowable, claims 7, 10 and 20 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after

allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art in view of Perera (U.S. 5,786,263).

Applicant admitted prior art teaches a method of semiconductor device fabrication using a semiconductor substrate comprising a lattice-strain relaxed silicon germanium layer (22) and a lattice strained silicon layer (24) formed in this order of mention onto a silicon substrate (21) (Fig. 4A-4C, pages 1-2). Applicant admitted prior art shows an etching step of etching the portions for device isolation regions of the semiconductor substrate to form device isolation regions (Fig. 4C, pages 1-2). Applicant admitted prior art discloses depositing a protective film for protecting portions for device activity regions onto the surface of the semiconductor substrate before the etching step (Fig. 4B).

Applicant admitted prior does not specifically show a deposition step of depositing a silicon film on the semiconductor substrate and an oxidation step of completely oxidizing the deposited silicon film. Applicant admitted prior does not specifically show

the silicon film having the thickness as claimed. However, Perera shows a deposition step of depositing a silicon film on the semiconductor substrate and an oxidation step of completely oxidizing the deposited silicon film (col. 2, lines 34-47). Perera teaches the silicon film having a thickness ranging from 5 to 60 nanometers (col. 2, lines 36-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Applicant admitted prior by including the steps of depositing a silicon film on the semiconductor substrate and completely oxidizing the deposited silicon film as taught by Perera in order to minimize the formation of voids in the isolation structures (Perera, col. 5, lines 10-15).

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al. (U.S. 5,847,419) in view of Perera (U.S. 5,786,263).

Imai et al. teaches a method of semiconductor device fabrication using a semiconductor substrate comprising a lattice-strain relaxed silicon germanium layer (15) and a lattice strained silicon layer (16) formed in this order of mention onto a silicon substrate (Fig. 3D, col. 4, lines 55-65, col. 8, lines 37-45). Imai et al. shows an etching step of etching the portions for device isolation regions of the semiconductor substrate to form device isolation regions (Fig. 3G, col. 8, lines 54-67). Imai et al. discloses using a semiconductor substrate comprising a lattice-strain relaxed silicon germanium layer, one or more semiconductor layers and a lattice strained silicon layer formed in this order of mention onto a silicon substrate (Fig. 9A-11C, col. 11, lines 64-67, col. 12, lines 1-51). Imai et al. shows depositing a protective film for protecting portions for device

activity regions onto the surface of the semiconductor substrate before the etching step (Fig. 3F-3G, col. 8, lines 54-60).

Imai et al. does not specifically show a deposition step of depositing a silicon film on the semiconductor substrate and an oxidation step of completely oxidizing the deposited silicon film. Imai et al. does not specifically show the silicon film having the thickness as claimed. However, Perera shows a deposition step of depositing a silicon film on the semiconductor substrate and an oxidation step of completely oxidizing the deposited silicon film (col. 2, lines 34-47). Perera teaches the silicon film having a thickness ranging from 5 to 60 nanometers (col. 2, lines 36-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Imai et al. reference by including the steps of depositing a silicon film on the semiconductor substrate and completely oxidizing the deposited silicon film as taught by Perera in order to minimize the formation of voids in the isolation structures (Perera, col. 5, lines 10-15).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Liou et al. (U.S. 5,130,268) and Jun (U.S. 5,915,191) teach the step of depositing a silicon film an oxidizing the silicon film as well known in the art. Xiang (U.S. 6,600,170), Chu et al. (U.S. 5,963,817), Herbots et al. (U.S. 5,241,214), Wang et al. (U.S. 5,155,571), and Hsu et al. (U.S. 6,583,000) show several embodiments related to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 8, 2004

María Guerrero

MARIA F. GUERRERO
PRIMARY EXAMINER